**ECEN 248 - Lab Report**

**Lab Number: 4**

**Lab Title: Simple Arithmetic Logic Unit**

**Section Number: 519**

**Student’s Name:** [Alex Allahar](mailto:alex.allahar@tamu.edu)

**Student’s UIN: 928009686**

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**TA: Yi Deng**

**Objectives:**

The purpose of this lab is to design ALU. Starting with an Add/Sub unit, and introducing a MUX. This circuit will also introduce two complements of arithmetic.

**Design:**

Design the Add/Sub unit shown in the lab 4 demo. Test the unit’s ability to add and subtract, by outputting to LEDs. Once this is functional, design the MUX as shown in the lab 4 demo. Test the MUX with LEDs to ensure it is operating correctly. Implement the outputs of SUMs and ANDs into the MUX. Test the ALU by connecting the MUX outputs, “Rs”, to LEDs.

**Conclusion:**

In this lab, I built an ALU. The Add/Sub unit used familiar gates but introduced two complement arithmetic. Next, the MUX was a new logic gate to use; however, this lab was able to demonstrate its purpose in a circuit design.

**Post-lab Deliverables:**

| c1 | c2 | OP | A | B | Result | Overflow |
| --- | --- | --- | --- | --- | --- | --- |
| 0 | 0 | AND | 0100 | 0110 | 0100 | N |
| 0 | 1 | AND | 0110 | 1101 | 0100 | N |
| 1 | 0 | ADD | 0100 | 0110 | 1010 | N |
| 1 | 0 | ADD | 0100 | 1101 | 0001 | Y |
| 1 | 0 | ADD | 1101 | 1001 | 0110 | Y |
| 1 | 1 | SUB | 0100 | 0111 | 1101 | N |
| 1 | 1 | SUB | 0110 | 1001 | 1101 | N |

1. The maximum gate delay for the ALU was 5 units. Starting from two inputs such as c1 and b1 going to the XOR then to the Add/Sub, then to the MUX. This is the longest delay assuming each logic gate has the same delay rate.
2. Overflow detection schematic

This design checks if the CarryIn and CarryOuts are different or the same. If they are different an output of 1 is shown in the overflow. This checks that two positive inputs give a positive output or vice versa with negative inputs.

